GW8316

6-Channel Proximity Sensor for SAR Applications

1 Description

The GW8316 is an advanced 6-channel capacitive sensor MCU designed specifically for SAR (Specific Absorption Rate) applications. Capable of high-performance proximity detection based on capacitive sensing circuit operating with a wide range 2.7 V ~ 3.6 V supply voltage, this intelligent and smart sensor excels the presence detection of a user at various distances. With the human body proximity detection ability of the GW8316, radio frequency (RF) emission power can be optimized in the presence of the human body. The GW8316 provides noticeable performance benefits to portable electronic devices manufacturers by helping them to comply with stringent electromagnetic radiation regulations and SAR standards.

The GW8316 communicates to a host over the Inter-Integrated Circuit(I²C) serial bus, which can solely operate even in sleep mode. The Host can wake up the device from sleep mode with an I²C command. The interrupt signal output can be activated to allow the host to get the relative proximity distance or to receive a detection notification in an efficient way.

Equipped with an on-chip calibration functionality, the GW8316 can maintain performance across a wide range of temperatures, humidity, and noisy conditions. This feature allows for regular sensitivity adjustments, simplifying product development and improving overall performance.

2 Features

- Flexible 2.7 V ~ 3.6 V supply voltage
- High performance capacitive sensing circuit
  - 6 capacitive sensing inputs
  - Capacitance resolution: 1 aF
  - Capacitance offset compensation: ~ 300 pF
  - Automatic offset capacitance calibration
  - Active shield driver
  - Temperature sensor for compensation
- 8051 compatible MCU core
  - 32 KB Flash, 3KB SRAM
  - Capacitive sensor control interface
    - Separate configurations per channel
    - Digital sensor status output
  - Dedicated digital signal processing core
  - Peripherals
    - 2 Timer, 1 WDT
    - 2 I²C serial interfaces, 1 UART
    - DMA
    - GPIO
    - 2 PWM
    - External interrupt output
  - Flexible Event/Status Handling
- Low power consumption
  - Active mode: 50 μA
  - Sleep mode: 1.9 μA

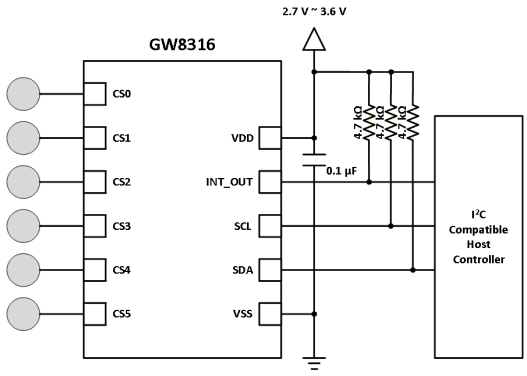
3 Physical Characteristics

- Supply voltage: 2.7 V ~ 3.6 V
- Operating temperature: -40 °C ~ 105 °C
- 12 DFN: 1.8 mm x 2.1 mm, 0.4 mm pitch
- 16 QFN: 3.5 mm x 3.5 mm, 0.8 mm pitch
- Pb & Halogen Free, RoHS/WEEE compliant

4 Typical Applications

- Wireless portable devices
  - Smartphones/Tablets/Laptops
  - Hotspots
  - Others

5 Basic Application Diagram



6 Ordering Information

Device name	Package	Remark
GW8316ADQDR	1.8 mm x 2.1 mm, 0.4 mm pitch	12 DFN Consumer
GW8316ARRJRQ	3.5 mm x 3.5 mm, 0.4 mm pitch	16 QFN AEC-Q100

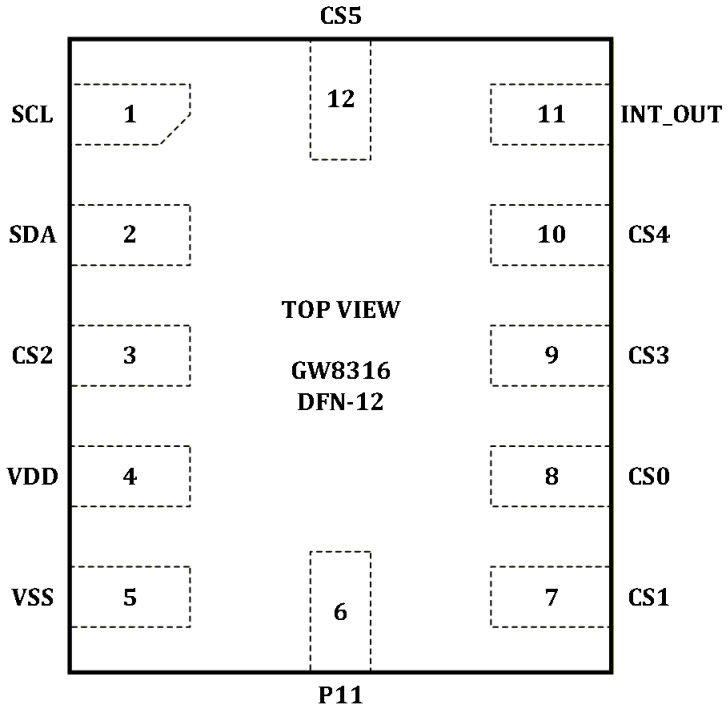
Table of Contents

7 Revision History

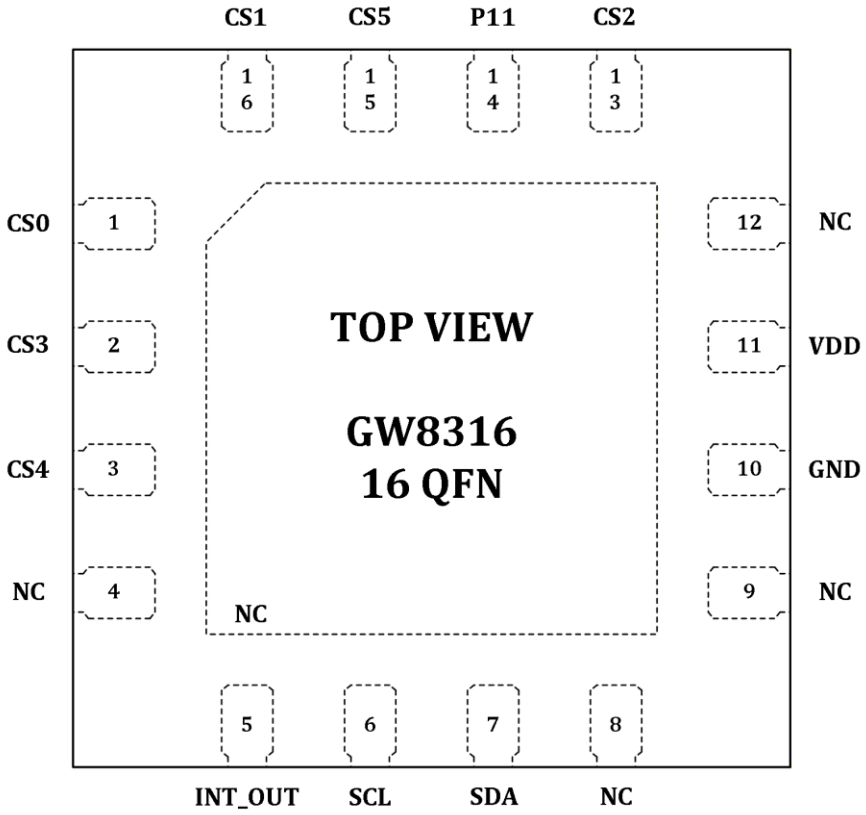
Version	Date	Description
1.0	December 2, 2025	Initial release

8 Pin Configuration and Function

12 DFN Package



16 QFN Package



Pin Description

Pin Name	12 DFN Pin No.	16 QFN Pin No.	Type	Description
P00 CS0 - - DSDA	8	1	IO	GPIO: Port0.0 AFE: Capacitive sensor input/Active shield output: channel 0 - - DBG: Debugger interface, serial data
P06 CS3 TIMER3_O PWM11_IO/OSCLS_O -	9	2	IO	GPIO: Port0.6 AFE: Capacitive sensor input/Active shield output: channel 3 TIMER3: interrupt output PWM1: PWM Port1, 1st output/input or 128 kHz internal oscillator output -
P07 CS4 UART_RX TIMER1_O/PWM01_IO -	10	3	IO	GPIO: Port0.7 AFE: Capacitive sensor input/Active shield output: channel 4 UART: RXD TIMER1: interrupt output or PWM0: PWM Port0, 1st PWM output/input -
NC	-	4	NC	No connection
P02 XINT0_IN UART_TX INT_OUT -	11	5	IO	GPIO: Port0.2 External interrupt 0 input UART: TXD Interrupt events open-drain output, external resistor required
P04 SSCL UART_TX SCL0 -	1	6	IO	GPIO: Port0.4 I²CS: Serial clock input UART: TXD I²C0: Serial clock input/output -
P03 SSDA UART_RX SDA0 -	2	7	IO	GPIO: Port0.3 I²CS: Serial data input, requires external 4.7 kΩ pull-up resistor UART: RXD I²C0: Serial data input/output, requires external 4.7 kΩ pull-up resistor -
NC	-	8	NC	No connection
NC	-	9	NC	No connection
GND	5	10	G	Power ground
VDD	4	11	P	Power supply; requires decoupling capacitors between VDD and GND
NC	-	12	NC	No connection
P05 CS2 SCLK_OUT OSCHS_O -	3	13	IO	GPIO: Port0.5 AFE: Capacitive sensor input/Active shield output: channel 2 System clock output 16 MHz internal oscillator output -
P11 - PWM12_O - EXCK_EN	6	14	IO	GPIO: Port1.1 - PWM1: PWM Port1, 2nd output - DBG: External clock input on/off selection, only for debugging
P10 CS5 PWM02_O - CLK_EXT	12	15	IO	GPIO: Port1.0 AFE: Capacitive sensor input/Active shield output: channel 5 PWM0: PWM port0, 2nd output - DBG: External clock input

Pin Name	12 DFN Pin No.	16 QFN Pin No.	Type	Description
P01 CS1 - - DSCL	7	16	IO	GPIO: Port0.1 AFE: Capacitive sensor input/Active shield output: channel 1 - - DBG: Debugger interface, serial clock
NC	-	17 Exposed Pad	NC	No connection

9 Specifications

9.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.5	5.5	V
Input Voltage	V_{IH}	-0.5	5.5	V
Operating Junction Temperature	T_{JCT}	-40	125	V
Storage temperature	T_{STG}	-55	150	℃
ESD HBM(ANSI/ESDA/JEDE JS-001)	ESD_{HBM}	8,000	-	V

9.2 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Supply Voltage(1)	V_{DD}	2.7(2)		3.6	V
Ambient Temperature	T_A	-40		105	℃

1. I²C/INT_OUT Pull-up resistors must not exceed the V_{DD} voltage level.
2. For optimal analog device performance, it is recommended that V_{DD} be equal to or greater than 2.7V.

9.3 Thermal Characteristics

Parameter	Symbol	Typical	UNIT
Thermal Resistance – Junction to Air (Static Airflow)(1)	θ_{JA}	TBD	℃/W

1. θ_{JA} is derived using a package situated in stationary air and affixed to a 3" x 4.5" 4-layer FR4 PCB, following JESD51 guidelines

9.4 DC Characteristics

Parameter	Symbol	MIN	TYP	MAX	UNIT
Input high voltage	V_{IH}	2.0		VDDA+0.3	V
Input high voltage, Schmitt trigger (V_{T+})	$V_{IH,SCH}$			2.1	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input low voltage, Schmitt trigger (V_{T-})	$V_{IL,SCH}$	0.7			V
Hysteresis ($V_{T+} – V_{T-}$)	V_{HYS}	0.2		1.4	V
Input high current, $V_{IN}=V_{DDA}$	I_{IH}	-10		10	μA
Input with pull-down, $V_{IN}=V_{DDA}$	$I_{IH,PD}$	80	100	125	μA
Input low current, $V_{IN}=V_{DDA}$	I_{IL}	-10		10	μA
Input with pull-up, $V_{IN}=V_{DDA}$	$I_{IL,PU}$	-80	-100	-125	μA

Parameter	Symbol	MIN	TYP	MAX	UNIT
Output high voltage	V_{OH}	2.4			V
Output low voltage	V_{OL}			0.4	V
3-State output leakage current	I_{OZ}	-10		10	μA

9.5 Internal DC Regulator Characteristics

Parameter	Symbol	MIN	TYP	MAX	UNIT
Internal digital LDO supply voltage	V_{DDD}	1.35	1.5	1.65	V
Internal digital LDO supply current	I_{DDD}			15	mA
Power on reset lockout voltage	$V_{POR,LOCKOUT}$		2.13		V
Power on reset release voltage	$V_{POR,RELEASE}$		2.27		V
Power on reset delay	$V_{POR,DELAY}$			1.2	ms

9.6 Electrical Characteristics

Unless stated otherwise, all values are applicable within the complete range of operational conditions. Typical values are given for T_A = + 25 °C , V_{DD} = 3.3 V

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Power Supply						
Active	I_{ACTIVE}	Scan Period = 30 ms Clock Frequency = 200 kHz Oversample = 64 CVC Gain = 4 ADC Gain = 1 DSP Disabled I²C listening. No load		50		μA
Doze	I_{DOZEI}	Scan Period = 390 ms Clock Frequency = 200 kHz Oversample = 64 CVC Gain = 4 ADC Gain = 1 DSP Disabled I²C listening. No load		8		μA
Sleep	I_{SLEEP}	Power down I²C listening		1.9		μA
Capacitance to Voltage Converter (CVC) + ADC						
Active Current	I_{ACTIVE}			600		μA
Power Down Current	I_{PD}			0.2		μA
External DC Capacitor to Ground	C_{EXT}				300	pF
Input Capacitance Range	C_{RANGE}		±1.05		±8.1375	pF
Measurement Range Control Step	$C_{RANGE,STEP}$			±0.2625		pF
Offset Cancellation DAC Resolution	$N_{BIT,DAC}$			14		Bits
CVC/ADC Sampling	$F_{Sampling}$		7.8125	250	500	kHz

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Frequency						
ADC Oversampling Ratio	OSR		1	32	512	
Measurement Resolution	N_{BIT}	C_{RANGE} = ±1.05, ADC Gain = 1		21		Bits
	C_{RES}	Default Gain		1		aF
Output Resolution	N_{BIT}	12 + $\log_2$(OSR)	12		21	bits
Oscillators						
Nominal Oscillator Frequency, Fast	$F_{OSC,FAST}$			16		MHz
Nominal Oscillator Frequency, Slow	$F_{OSC,SLOW}$			128		kHz
Oscillator Trim Step	OSC_{TRIM}	Around Nominal Value T_A = + 25 °C , V_{DDA} = 3.3V		0.65		%
Oscillator Temperature Dependency	OSC_{TEMPD}			±2		%

9.7 Timing Diagrams

9.7.1 I²C Timing Diagrams

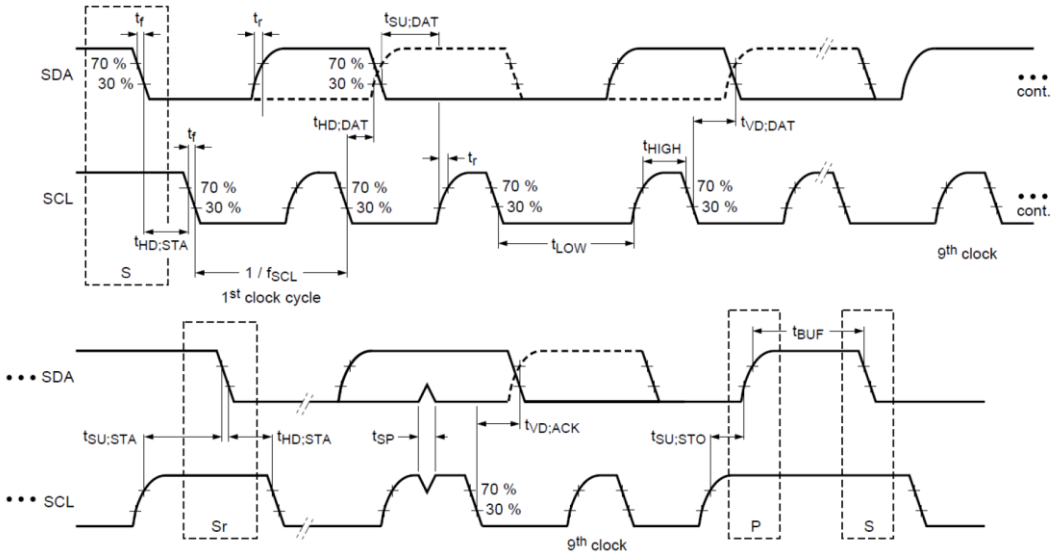


Figure 1 I²C Timing Diagram

Table 1 I²C Timing Parameters

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
SCL clock frequency	t_{SCL}				400	kHz

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
SCL low period	t_{LOW}		1.3			μs
SCL high period	t_{HIGH}		0.6			μs
Data setup time	t_{SUDAT}		0.1			μs
Data hold time	t_{HDDAT}		0			μs
Repeated start setup time	t_{SUSTA}		0.6			ns
Start condition hold time	t_{HDSTA}		0.6			μs
Stop condition setup time	t_{SUSTO}		0.6			μs
Bus free time between stop and start	t_{BUF}		1.3			μs
Data valid time	t_{VDDAT}				0.9	μs
Data valid acknowledge time	t_{VDACK}				0.9	μs
Rise time of SCL	t_{rCL}		20		300	ns
Fall time of SCL	t_{fCL}		$20*(V_{DD}/5.5)$		300	ns
Rise time of SDA	t_{rDA}		20		300	ns
Fall time of SDA	t_{fDA}		$20*(V_{DD}/5.5)$		300	ns
Input glitch suppression	t_{SP}	See note 1	0		50	ns

Notes:
[1] Minimum glitch amplitude is $0.7V_{DD}$ at high level and maximum $0.3V_{DD}$ at low level

10 Functional Description

10.1 Overview

The GW8316 is an advanced 6-channel capacitive sensor MCU for Specific Absorption Rate (SAR) applications. Capable of high-performance proximity detection based on capacitive sensing circuit operating with a wide range 2.7 V ~ 3.6 V supply voltage, this intelligent and smart sensor excels the presence detection of a user at various distances. With the human body proximity detection ability of the GW8316, radio frequency (RF) emission power can be optimized in the presence of the human body. The GW8316 provides noticeable performance benefits to portable electronic devices manufacturers by helping them to comply with stringent electromagnetic radiation regulations and SAR standards.

With the GW8316, users can implement fully customized proximity sensing functions such as periodical sensing with environmental variation compensation. Simple register based control structure supports efficient Active Mode/Doze Mode/IDLE Mode implementation for power optimized operations.

Equipped with an on-chip calibration functionality, the GW8316 can maintain performance across a wide range of temperatures, humidity, and noisy conditions. This feature allows for regular sensitivity adjustments, simplifying product development and improving overall performance.

The GW8316 communicates to a host over the Inter-Integrated Circuit (I^2C) serial bus, which can solely operate even in sleep mode. The host can wake up the device from sleep mode with an I^2C command. The interrupt signal output (INT_OUT) can be activated to allow the host to get the relative proximity distance or to receive a detection notification in an efficient way.

10.2 Functional Block Diagram

Figure 2 illustrates the functional block of the GW8316.

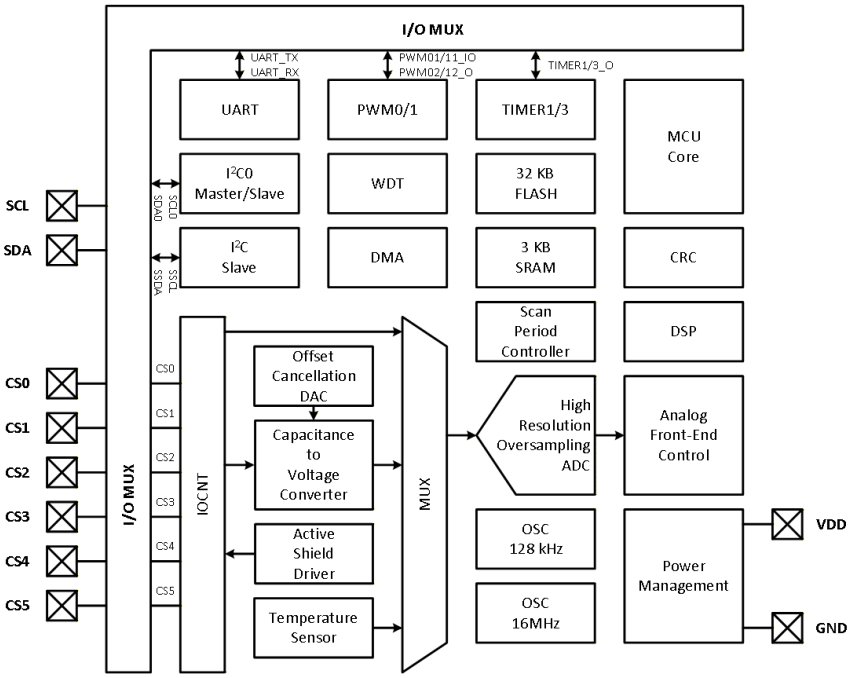


Figure 2 Functional Block Diagram

10.3 Proximity Sensing Interface

10.3.1 Introduction

The primary role of the proximity sensing interface is to identify the presence of a conductive object, often a part of the human body like a finger, palm, or face, in close proximity to the system as relative parasitic capacitance changes to the ground. Capacitive proximity sensing is widely used due to its accuracy and versatility. The GW8316 capacitive proximity sensing structure is illustrated in the figure.

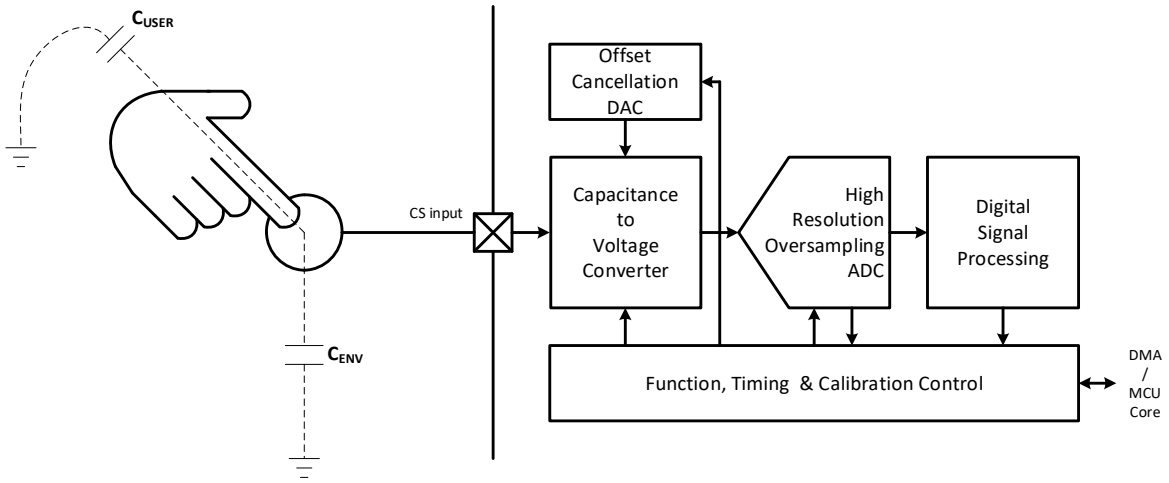


Figure 3 Proximity Sensing Interface

The sensor could be as straightforward as a copper region on a PCB or FPC. As a conductive object comes close and moves, its capacitance (to ground) will change accordingly.

The GW8316's Analog Front-End (AFE) circuit including Capacitance to Voltage Converter (CVC), Offset Cancellation DAC/High Resolution Oversampling ADC/Digital Signal Processing/Function, Timing & Calibration Control blocks co-works with MCU core to control and process capacitive proximity sensor data. Users can directly set each control register or simple register-based command can load preset values for each channel to registers. Users can turn on/off internal blocks in predefined settings or can directly turn on/off each block. Dedicated scan period controller block generates interrupts in defined periods on MCU for each channel. With these blocks, users can implement fully customized proximity sensing functionality in efficient ways.

The AFE handles the direct measurement and compensation of the sensor's capacitance and provide signals to the high-resolution oversampling analog to digital converter (ADC).

ADC translates it into a digital format. The digital processing block calculates the capacitance measurement received from the ADC and derives binary proximity status data, whether the distance to the object is over threshold or under threshold.

The control block initiates and adjust the AFE and the ADC operations like sampling rate, capacitance calibration, and send result data to memory via DMA or MCU core.

The GW8316 offers complete customization of sensor sensitivity, detection thresholds, and etc. Capacitive proximity detection relies on the internal gain and sampling frequency settings of the GW8316, as well as the size of the external sensor, to achieve optimal proximity detection distance. For example, to extend the proximity detection range without altering the capacitive sensor's dimensions, a high sensitivity setting and/or lower signal threshold setting for proximity detection can be used. GW8316 supports a command to load preset configuration for each channel directly.

10.4 Analog Front End (AFE)

10.4.1 Capacitance Sensing

Capacitive sensing involves detecting slight changes in capacitance within a noisy environment. As mentioned earlier, the proximity sensing interface of the GW8316 is based on capacitive sensing technology. In instances where the target conductive object (finger/palm/face, etc.) is absent, the sensor exclusively detects an inherent capacitance value, denoted as C_{env}. This capacitance emerges due to the interaction of the sensor's electrical field with its environment, notably with ground regions. Upon the approach of the conductive object (finger/palm/face, etc.), the sensor's electric field experiences alteration, leading to a rise in the overall capacitance sensed by the sensor due to the user capacitance, C_{user}.

$$C_{sensor} = C_{env} + C_{user}$$

The complexity in capacitive sensing lies in identifying the relatively minor change in C_{sensor} (with C_{user} typically accounting for only a small percentage). This differentiation must occur against the background of environmental noise (C_{env}), which changes gradually alongside environmental factors like temperature. To address this, the GW8316 incorporates an capacitance compensation DAC. This DAC eliminates the C_{env} element on the circuit by extracting and processing solely the C_{user} component. This method leads to the highest level of robustness and efficiency.

10.4.2 CS Input and Active Shield Driver

10.4.3 AFE Block Diagram

The GW8316's AFE incorporates a Capacitance to Voltage Converter (CVC), responsible for sensing the sensor's capacitance and transforming it into a voltage signal for further processing. Additionally, it encompasses an offset compensation circuit, and a high-resolution oversampling ADC.

10.4.4 Capacitance to Voltage Conversion (C-V)

The Capacitance to Voltage Converter interfaces capacitance and sample input in defined sampling frequency and generates voltage output. The sensitivity of the interface is predominantly established by the sampling frequency and gain parameter.

10.4.5 Capacitance Compensation

Capacitance compensation involves conducting a singular measurement of C_{env}, which is then subtracted from the overall capacitance C_{sensor}. This was achieved by the capacitance compensation DAC removing the effect of C_{env} on CVC circuit. This action ensures that the ADC receives only the nearest contribution of C_{user}, effectively isolating it from C_{sensor}.

10.4.6 Analog to Digital Conversion (ADC)

A high-resolution oversampling Analog-to-Digital Converter (ADC) is employed to transform the analog capacitance data into digital. Users can adjust the resolution of the ADC from 12 bit to 21 bit, which is affected by the setting of the Over-Sampling Ratio (OSR) of ADC. Be aware that the OSR and sampling frequency of ADC directly affect the bandwidth of the converted signal.

10.4.7 Scan Period Controller

For power conservation and considering the inherently gradual occurrence of proximity events, the GW8316 supports to awaken periodically at a predefined scan interval. The scan period counter (SPC) block generates interrupts in user preset periods for each channel. There are 2 different period types which can be selected by simple register setting supporting users can implement Active/Doze Mode. The SPC is implemented with a dedicated lower power 128 kHz oscillator clock.

Users can freely implement environment compensation, proximity sensing and then put devices into idle state as depicted in the diagram below.

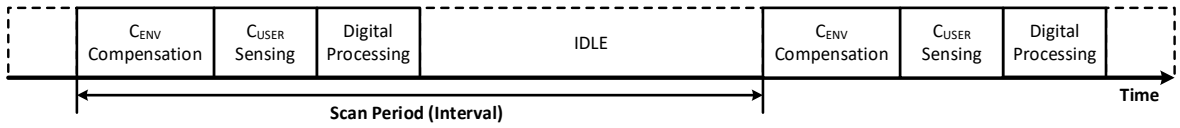


Figure 4 Sequencing of Proximity Sensing

The scan period establishes the minimum response time and can be programmed within the typical range of 0.5 ms to 32.768 s.

The reaction time of SAR detection is directly related to the scan period and inversely related to power consumption such that longer scan periods result in lower power consumption but also lead to longer detection reaction times. For example, users may implement the Active/Doze Mode Switching Concept like below. The GW8316 supports automatic period switching based on the detection result.

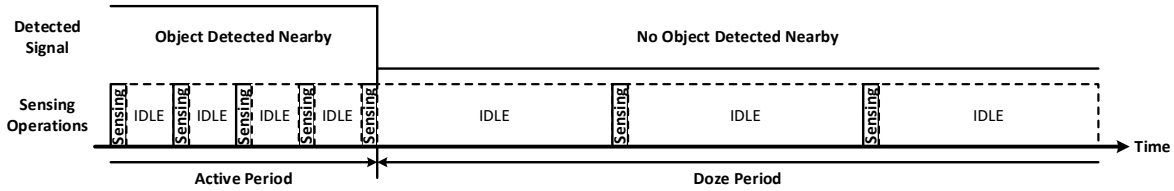


Figure 5 Active/Doze Mode Switching Scheme

10.5 Digital Signal Processing

The GW8316 includes dedicated high resolution digital signal processing (DSP) block which supports basic operations like ADD, SUBSTRACT, MULTIFLY, LEFT/RIGHT SHIFT, COPY, and COMPARE. The DSP block also supports more sophisticated operations like MAC OPERATION, AVERAGE, LOW PASS FILTER. Users can implement the user's own additional digital signal processing functions to enhance signal clarity or to extract additional information in real-time.

10.6 Host Communication

The GW8316 supports two types of serial communication – I²C serial bus and UART. To notify data/information ready to the host in efficient ways, interrupt output on a PAD can be used with these. Various interrupt sources can be forwarded to the PAD output including sources from proximity sensing block like CONV_DONE, COMP_DONE, DETECT, etc. This makes it possible to reduce the host's resources usage for checking the proximity sensor periodically. I²C serial bus can operate solely in sleep mode. Hosts can wake up the GW8316 with a single I²C command.

Users may make the GW8316 response to host at various proximity conditions. These conditions include:

1. Close Detection (In Range): An interrupt can be triggered when the sensor detects that the user is in close proximity or within the defined range.

2. Far Detection (Out of Range): Alternatively, an interrupt can be triggered when the sensor detects that the user is far away and outside the designated range.

3. Both Close and Far Detection: In some cases, the interrupt can be configured to trigger for both close and far detection scenarios. This means that the interrupt can be activated when the user enters or exits the specified range.

An interrupt can serve another purpose as well—it can be triggered at the conclusion of every conversion within a scan period. This particular interrupt provides the host with a signal indicating that the proximity sensing block is actively in operation.

The host can leverage this signal for several purposes:

1. Synchronization of Noisy System Operations: In situations where the system's operations may introduce noise or timing uncertainties, the interrupt helps in synchronizing activities. By knowing when each conversion cycle is complete, the host can coordinate its actions with the sensing block more effectively, minimizing interference and ensuring reliable operation.

2. Synchronous Reading of Phase Data: The host can utilize this interrupt to read phase data (signal on different channels) synchronously. Synchronous reading ensures that the data is acquired at precisely the right moment, allowing the host to monitor and process proximity-related information accurately. This is particularly valuable for applications that demand real-time proximity data analysis and decision-making.

In summary, the interrupt serves as a synchronization tool, providing the host with a signal indicating the status of the proximity sensing block's conversions. This allows the host to manage system operations effectively, synchronize tasks, and access phase data in a synchronized manner for monitoring and control purposes.

In addition to the examples mentioned earlier, the interrupt functionality offers versatility by allowing mapping to various status bits, tailored to meet specific application requirements. One can refer to the register map for detailed information regarding how the interrupt can be customized and mapped to suit any needs of applications

10.7 Power Controls

The GW8316 gives sufficient controllability to users to implement power/performance optimized characteristics. There are 5 power status defined in GW8316; Wait for Interrupt (WFI) #1, Wait for Interrupt (WFI) #2, IDLE, SLEEP, STOP, where wait for interrupt is the status MCU stops further instruction fetch or execution and just wait for an interrupt. Users can simply set PCON_CMD to transit into required power status. When PCON_CMD changes, block power control sequences are automatically performed.

Power Modes

Power State	MCU	MCU CLOCK	SYSTEM CLOCK	FLASH	16 MHz Oscillator	LDO	128 kHz Oscillator
WFI1	Waiting for Interrupt	On	On	On	On	Normal Mode	On
WFI2	Waiting for Interrupt	Off	On	On	On	Normal Mode	On
IDLE	Waiting for Interrupt	Off	Off	Off	On	Normal Mode	On
SLEEP	Waiting for Interrupt	Off	Off	Off	Off	Low Power	On
STOP	Waiting for Interrupt	Off	Off	Off	Off	Low Power	Off

10.8 I²C Interface

10.8.1 Introduction

The I²C implementation of the GW8316, utilized by the host for communication, is:

- Two I²C interface: I²C0 support master/slave mode, I²CS only support slave mode
- Standard (100kbps) and Fast (400kbps) modes
- 7-bit address, configurable by a resistor
- General call support

I²CS supports external wake-up. Because I²CS uses SCL as its clock, the host can wake-up the MCU core even when the internal oscillator is powered down in SLEEP or STOP mode. Whenever one byte is transferred by I²C bus, an interrupt is generated to the MCU core and the SCL is held low until the register is cleared.

Users can directly control generation of START/STOP condition, read/write data, and ACK generation. The GW8316 I²C report various bus status like address matching, bus busy, etc. These functions enable users to implement customized protocols efficiently.

10.9 Registers

The following registers provide comprehensive scope for user-driven parameter customization. It's crucial to configure their values in alignment with the most recent application notes accessible (kindly consult your Gwanak Analog representative).

Please take note of the following:

- Addresses not explicitly mentioned are reserved and should not undergo any writing operation.
- Any reserved bits should be retained at their default values unless explicitly directed otherwise.
- Unless specifically indicated otherwise, default values can be perceived as typical standards.

SFR Registers

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
System Control Registers											
SP		Stack Pointer	0x07								
DPL		Data Pointer Low	0x00	DPTR[7:0]							
DPH		Data Pointer High	0x00	DPTR[15:8]							
SYSCON_AR		System Authority	0x00	AR							
SYSCON		System Control	0x1D	CPP_CTRL_EN	-	-	OSCLS_PDB	OSCHS_PDB	LDO_PDB	SUBLDO_PDB	CDB_EN

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SCCR		System Clock Control	0x0C	-	PCLK_DIV_EN	-	-	SCLK_SEL		SCLK_SRC_DIV_DIS	SCLK_SRC_SEL
PCON		Power Control LDO_EN: “1” Do not power down LDO in SLEEP or STOP FLASH_EN: “1” Do not power down Flash in IDLE, SLEEP or STOP PCON_CMD: Power controller command 0: Wait for Interrupt 1 1: Wait for Interrupt 2 2: IDLE 3: SLEEP 4: STOP Others: Wait for Interrupt 1	0x00	-	-	-	LDO_EN	FLASH_EN	PCON_CMD		
DPTR_BANK	R W	MCU DPTR Register Bank Selection (Two Banks)	0x00	-	-	-	-	-	-	-	MCU_DPTR
XBANK			0x00								
XOFFSET			0x00								
PSW			0x00								
ACC			0x00								
B			0x00								
CMX			0x00								
SUB_CLKEN_H	R W	Sub-block Clock Enable High	0x08	-	-	PWM1	PWM0	I2CS	I2C0	-	UART0
SUB_CLKEN_L	R W	Sub-block Clock Enable Low	0x10	-	AFEC	DSP	FC	CRC	-	-	-
SUB_RESET_H	R W	Sub-block Reset High	0x00	-	-	PWM1	PWM0	I2CS	I2C0	-	UART0
SUB_RESET_L	R W	Sub-block Reset Low	0x00	-	AFEC	DSP	FC	CRC	TIMER3	TIMER1	-
CHIPID_3	R O	CHIPID	0x00	CHIPID[31:24]							

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CHIPID_2	R O		0x83	CHIPID[23:16]							
CHIPID_1	R O		0x10	CHIPID[15:8]							
CHIPID_0	R O		0xA0	CHIPID[7:0]							
INTERRUPT Registers											
INT_OFFSET	R W	Interrupt Vector Base Address	0x00	IVS[15:8]							
XINT_EDGE	R W	Ext interrupt, edge interrupt enable configuration for XINT[0]	0x00	-	-	-	NEG_EN	-	-	-	POSEN
XINT_SR	R W	Ext. interrupt status for XINT[0]	0x00	-	-	-	NEG_ST	-	-	-	POS_ST
IRQ0	R W	Interrupt Request 0	0x00	-	-	UART0	AFEC	-	I2C0	-	-
IEN0	R W	Interrupt Enable 0	0x00	INT_EN_GLOBAL	INT_EN_LOCAL[6:0]						
IP0	R W	Interrupt Priority 0	0x00	0	INT_PRIORITY[6:0]						
IRQ1	R W	Interrupt Request 1	0x00	WDT	TIMER1	-	-	I2CS	EXT	TIMER3	3
IEN1	R W	Interrupt Enable 1	0x00	INT_EN_LOCAL[14:7]							
IP1	R W	Interrupt Priority 1	0x00	INT_PRIORITY[14:7]							
IRQ2	R W	Interrupt Request 2	0x00	-	-	SPC	DMA RX	DMA TX	-	PWM1	PWM2
IEN2	R W	Interrupt Enable 2	0x00	INT_EN_LOCAL[22:15]							
IP2	R W	Interrupt Priority 2	0x00	INT_PRIORITY[22:15]							
ILEVEL	R W	Current Interrupt Level	0x00	-	-	-	-	-	LEVEL[2:0]		

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
GPIO Registers											
P0	R W	GPIO P07 ~ P00	0x00	P07	P06	P05	P04	P03	P02	P01	P00
P1	R W	GPIO P17 ~ P10	0x00	P17	P16	P15	P14	P13	P12	P11	P10
I²C0 Registers											
I2C0_CSR	W	I2C0 Command Status	0x00	STA	STO	RD	WR	ACK	-	-	IACK
	R		-	RxACK	TMOUT	AL	CMDF	ADMF	GCMF	STDF	IF
I2C0_CTRL	W R	I2C0 Control I2C_EN, IEN: Write Only BUSY, TOP: Read Only	0x00	I2C_EN	IEN	MASTER	-	-	-	BUSY	TIP
I2C0_PRER	R W	I2C0 Pre-divider I2C0 Freq. = SCLK Freq. / (5 * (PRER + 1))	0x00	PRER							
I2C0_ADDR	R W	I2C0 Device Address	0x00	DEVADDR							GC
I2C0_DR	R W	I2C0 Data	0x00	DATA							
I2C0_TOR	R W	I2C0 Time-out Value	0x00	TOR							
I2CS_CSR	W	I2CS Command and Status	0x00	-	-	-	-	-	-	-	IACK
	R		0x00	RXACK	-	-	BDF	ADMF	GCMF	STDF	-
I2CS_ADDR	R W	I2CS Slave Address	0x40	SLV_ADDR							GC
I2CS_CFG	R W	I2CS Configuration	0x7F	-	STRETCH_RLAST	WE_BDF	WE_ADMF	WE_STDF	IE_BDF	IE_ADMF	IE_STDF
I2CS_DR	R W	I2CS Data	0x00	DATA							

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
I2CS_SDA_DLY	R W	I2CS Delay Configuration	0x00	-	-	-	-	SDA_ODLY		SDA_IDLY	
PWM Registers											
PWM0_PRED	R W	PWM0 Pre-divider	0x00	INTDIS	MEAS	PRED[5:0]					
PWM0_PLSPL	R W	PWM0 Pulse Period	0x00	PLSP[7:0]							
PWM0_MODE	R W	PWM0 Mode	0x00	EN	OPOL	MODE	PLSP[12:8]				
PWM0_PLSW1L	R W	PWM0 Pulse Width 1	0x00	PLSW1[7:0]							
PWM0_PLSW1H	R W	PWM0 Pulse Width 1	0x00	-	-	-	PLSW1[12:8]				
PWM0_PLSW2L	R W	PWM0 Pulse Width 2	0x00	PLSW2[7:0]							
PWM0_PLSW2H	R W	PWM0 Pulse Width 2	0x00	-	-	-	PLSW2[12:8]				
PWM1_PRED	R W	PWM1 Pre-divider	0x00	INTDIS	MEAS	PRED[5:0]					
PWM1_PLSPL	R W	PWM1 Pulse Period	0x00	PLSP[7:0]							
PWM1_MODE	R W	PWM1 Mode	0x00	EN	OPOL	MODE	PLSP[12:8]				
PWM1_PLSW1L	R W	PWM1 Pulse Width 1	0x00	PLSW1[7:0]							
PWM1_PLSW1H	R W	PWM1 Pulse Width 1	0x00	-	-	-	PLSW1[12:8]				
PWM1_PLSW2L	R W	PWM1 Pulse Width 2	0x00	PLSW2[7:0]							
PWM1_PLSW2H	R W	PWM1 Pulse Width 2	0x00	-	-	-	PLSW2[12:8]				
DSP Registers											
DSP_CON	W	DSP Control	-	-	-	-	-	-	-	-	LE

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	R		0x08	BUSY	0	0	0	ADD_ZERO	ADD_NEG	ADD_POS	LE
DSP_CMD	R W	DSP Command	0x00	OP_CODE			XSEL		YSEL		ZSTORE
DSP_DPTR	R W	DSP DMA Bank Selection	0x00	DPTR_BANK							
DSP_SHIFT	R W	DSP Shift Amount	0x00	-	-	-	SFT_N				
DSP_DWIDTH	R W	DSP Data Width	0x15	-	-	X_LEN		Y_LEN		Z_LEN	
DSP_XPTR	R W	DSP Operand X Pointer	0x00	PTR[7:1]							XCONST
DSP_YPTR	R W	DSP Operand Y Pointer	0x00	PTR[7:1]							YCONST
DSP_ZPTR	R W	DSP Result Z Pointer	0x00	PTR[7:1]							0
UART Registers											
UART0_CSR	R W	UART0 Control and Status	0x00	INTM	EN	PS		FBRE	SL	TX_BRK	ABRE
UART0_ISR	R W	UART0 Interrupt Status	0x00	SYNCDET	TF_EMPTY	RF_FULL	RF_READY	BRKDET	PE	FE	OVR
UART0_IBRD	R W	UART0 Baud Rate Divider	0x00	PCLK_SEL				CLK_DIV			

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
UART0_DR	R W	TX/RX Data	0x00	DATA							
UART0_FBRD	R W	Fractional Baud Rate Divider	0x00	FBRD[7:0]							
TIMER Registers											
T1MR	R W	Timer1 Mode Control	0x00	PCLK_SEL					RD_CNT	ME	EN
T1RL	R W	Timer1 Time	0x00	T1R[7:0]							
T1RH	R W	Timer1 Time	0x00	T1R[15:8]							
WDTMR	R W	Watch Dog Timer Mode	0x00	PCLK_SEL					CLK	RESET	EN
WDTR	R W	Watch Dog Timer Time	0x00								
T3MR	R W	Timer3 Mode Control	0x00	PCLK_SEL					RD_CNT	ME	EN
T3RL	R W	Timer3 Time	0x00	T3R[7:0]							
T3RH	R W	Timer3 Time	0x00	T3R[15:8]							
SPC Registers											
SPC_CSR	R W	Scan Period Control and Status	0x00	INT_STATE	PAUSE_CDC	EN_CDC	MATCH_BW	INT_EN	INT_ON_GSP	PAUSE	EN
SPC_MATCH	R	If MATCH_BW=0, Scan Period Expiration Status of Each Channel	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
	R	If MATCH_BW=1, Scan Period Expiration Status of Current Channel	0x00	-	-	-	-	-	-	-	MATCH
CRC Registers											
CRC_CON	R W	CRC Control	0x00	TARGET				TYPE		0	EN
CRC_DIN	R W	CRC Data	0x00	DIN[7:0]							

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CRC_L	R W	CRC Low	0x00	CRC[7:0]							
CRC_H	R W	CRC High	0x00	CRC[15:8]							

XSFR Registers

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
GPIO Registers											
P0PINMUX_H	R W	GPIO Port 0 Pinumx P07 ~ P04	0x50	P07		P06		P05		P04	
P0PINMUX_L	R W	GPIO Port 0 Pinumx P03 ~ P00	0x00	P03		P02		P01		P00	
P1PINMUX_H	R W	GPIO Port 1 Pinumx P17 ~ P14	0x00	P17		P16		P15		P14	
P1PINMUX_L	R W	GPIO Port 1 Pinumx P13 ~ P10	0x00	P13		P12		P11		P10	
P0_DS_H	R W	GPIO Port 0 Driving Strength Control P07 ~ P04	0xAA	P07		P06		P05		P04	
P0_DS_L	R W	GPIO Port 0 Driving Strength Control P03 ~ P00	0xAA	P03		P02		P01		P00	
P1_DS_H	R W	GPIO Port 0 Driving Strength Control P17 ~ P14	0x00	-		-		-		-	
P1_DS_L	R W	GPIO Port 0 Driving Strength Control P13 ~ P10	0x0A	-		-		P11		P10	
P0_DIR	R W	GPIO Port 0 direction control	0x00	P07	P06	P05	P04	P03	P02	P01	P00
P1_DIR	R W	GPIO Port 1 direction control	0x00	P17	P16	P15	P14	P13	P12	P11	P10
P0_PE	R W	GPIO Port 0 pull-up/down enable	0x00	P07	P06	P05	P04	P03	P02	P01	P00
P1_PE	R W	GPIO Port 1 pull-up/down enable	0x02	P17	P16	P15	P14	P13	P12	P11	P10
P0_PS	R W	GPIO Port 0 pull-up/down selection	0x00	P07	P06	P05	P04	P03	P02	P01	P00
P1_PS	R W	GPIO Port 1 pull-up/down selection	0x00	P17	P16	P15	P14	P13	P12	P11	P10
P0_DB	R W	GPIO Port 0 Debounce Filter on/off control	0x03	P07	P06	P05	P04	P03	P02	P01	P00
P1_DB	R W	GPIO Port 1 Debounce Filter on/off control	0x00	P17	P16	P15	P14	P13	P12	P11	P10
P0_DB_CNT	R W	GPIO Port 0 Debounce Filter Count Value	0x02	-	-	-	-	DB_CNT			
P1_DB_CNT	R W	GPIO Port 0 Debounce Filter Count Value	0x02	-	-	-	-	DB_CNT			

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SEL_CAPTURE	R W	Select Timer 1/3 Capture Signal Source SEL1: capture signal source for Timer 1, 0 – disable, 1 - P0[2], 2 – P[5], 3 – P[6] SEL3: capture signal source for Timer3, 0-disable, 1-P1[0], 2-OSCHS divided pulse, 3-OSCLS divided pulse	0x00	-	-	-	-	SEL3		SEL1	
PIN_XCHG	R W	Pin Exchange Control UART0: '1' exchanges UART_RXD/UART_TXD I2C0: '1' exchanges I2C0 SCL0/SDA0 I2CS: '1' exchanges I2CS SSCL/SSDA T1P1: '1' exchanges TIMER1_O/PWM01_IO outputs P11OSC: '1' exchanges PWM11_IO/OSCLS_O outputs	0x00	-	-	-	P11OSC	T1P01	I2CS	I2C0	UART0
DMA Registers											
DMA_CH2_SRC_H	R W	DMA Channel2 Source Address High Bits	0x00	-	-	SRC_PTR[13:8]					
DMA_CH2_SRC_L	R W	DMA Channel2 Source Address Low Bits	0x00	SRC_PTR[7:0]							
DMA_CH2_TX_CTRL	R W	DMA Channel2 TX Control	0x00	C_DMA_GO	C_N_MINUS_1[6:0]						
DMA_CH2_TXSEL	R W	DMA Channel2 TX Select	0x00	-	-	-	-	-	-	TX_SEL [1:0]	
DMA_CH2_DST_H	R W	DMA Channel2 Destination Address High Bits	0x00	-	-	DST_PTR[13:8]					
DMA_CH2_DST_L	R W	DMA Channel2 Destination Address Low Bits	0x00	DST_PTR[7:0]							
DMA_CH2_RXCTRL	R W	DMA Channel2 RX Control	0x00	C_DMA_GO	C_N_MINUS_1[6:0]						
DMA_CH2_RXSEL	R W	DMA Channel2 RX Select	0x00	-	-	-	-	-	-	RX_SEL [1:0]	
PWM Registers											
PWM_PLSW1_H	R O	PWM1 input pulse width	-	0			WIDTH[12:8]				
PWM_PLSW1_L	R O		-	WIDTH[7:0]							
PWM_PLSW2_H	R O	PWM2 input pulse width	-	0			WIDTH[12:8]				
PWM_PLSW2_L	R O		-	WIDTH[7:0]							
PWM_PLSW3_H	R O	PWM3 input pulse width	-	0			WIDTH[12:8]				

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PWM_PLSW3_L	R O		-	WIDTH[7:0]							
PWM_PLSW4_H	R O	PWM4 input pulse width	-	0			WIDTH[12:8]				
PWM_PLSW4_L	R O		-	WIDTH[7:0]							
PRX Registers											
INTOUT_SRC	R W	INT_OUT Pin Source RESET: '1' connects INT_RESET signal to INT_OUT DETECT: '1', 'connects INT_DETECT to INT_OUT RELEASE: if '1', 'proximity released' will forward to INT_OUT COMP_DONE: if '1', 'offset capacitance compensation done' status will forward to INT_OUT CONV_DONE: if '1', 'capacitance conversion done' status will forward to INT_OUT STARTUP_DET: if '1', 'proximity detected on start-up' status will forward to INT_OUT AUTO_SET: internal Int_detect, int_release, int_comp_done, and int_startup_det are loaded into INT_DETECT, INT_RELEASE, INT_COMP_DONE, and INT_STARTUP_DET respectively, and then cleared to 0 Int_detect is set to 1 when software sets DETECT1_BW from 0 to 1 Int_release is set to 1 when software ckears DETECT1_BW from 1 to 0 Int_comp_done is set to 1 when software clears COMP_PENDING_BW from 1 to 0 Int_sup_det is set to 1 when software sets (or clears) STARTUP_DET_BW from 0 to 1 (or 1 to 0)	0x00	RESET(READY)	DETECT	RELEASE	COMP_DONE	CONV_DONE	STARTUP_DET		AUTO_SET (WO)

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
INTOUT_EN	R W	INT_OUT Pin Source Enable RESET:'1' enables RESET interrupt DETECT:'1' enables DETECT interrupt RELEASE: '1' enables RELEASE interrupt COMP_DONE: '1' enables COMP_DONE interrupt CONV_DONE: '1' enables RESET: '1' connect INT_RESET signal to INT_OUT DETECT: if '1', 'proximity detected' status will forward to INT_OUT RELEASE: if '1', 'proximity released' will forward to INT_OUT COMP_DONE: if '1', 'offset capacitance compensation done' status will forward to INT_OUT CONV_DONE: if '1', 'capacitance conversion done' status will forward to INT_OUT STARTUP_DET: if '1', 'proximity detected on start-up' status will forward to INT_OUT	0x00	RESET(READY)	DETECT	RELEASE	COMP_DONE	CONV_DONE	STARTUP_DET	INT_OD	INT_POL
CUR_CH	R W	Current Channel Number	0x00	-	-	-	-	-	CUR_CH[2:0]		
DETECT1	R W	Proximity Detected, Threshold1	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
DETECT1_BW	R W	Proximity Detected, Threshold1, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
DETECT2	R W	Proximity Detected, Threshold2	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
DETECT2_BW	R W	Proximity Detected, Threshold2 Bit Wise	0x00	-	-	-	-	-	-	-	CH x
DETECT3	R W	Proximity Detected, Threshold3	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
DETECT3_BW	R W	Proximity Detected, Threshold3 Bit Wise	0x00	-	-	-	-	-	-	-	CH x
DETECT4	R W	Proximity Detected, Threshold4	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
DETECT4_BW	R W	Proximity Detected, Threshold4 Bit Wise	0x00	-	-	-	-	-	-	-	CH x
COMP_PENDING	R W	Comparator Output Pending	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
COMP_PENDING_BW	R W	Comparator Output Pending, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
STARTUP_DET	R W	Startup Detected	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
STARUP_DET_BW	R W	Startup Detected, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
INIT_PENDING	R W	Initialize Pending	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
INIT_PENDING_BW	R W	Initialize Pending, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
SCAN_PERIOD_0	R W	Scan Period for CH0/1	0x00	-	CH1			-	CH0		
SCAN_PERIOD_1	R W	Scan Period for CH2/3	0x00	-	CH3			-	CH2		
SCAN_PERIOD_2	R W	Scan Period for CH4/5	0x00	-	CH5			-	CH4		
-	R W	-	0x00	-	-			-	-		
DOZE_PERIOD_0	R W	Doze Period for CH0/1	0x00	-	CH1			-	CH0		
DOZE_PERIOD_1	R W	Doze Period for CH2/3	0x00	-	CH3			-	CH2		
DOZE_PERIOD_2	R W	Doze Period for CH4/5	0x00	-	CH5			-	CH4		
-	R W	-	0x00	-	-			-	-		
G_SCAN_PERIOD_H	R W	Global Scan Period upper bits	0x00	-	-	-	G_SCAN_PERIOD[12:8]				
G_SCAN_PERIO_L	R W	Global Scan Period lower bits	0x00	G_SCAN_PERIOD[7:0]							
CH_EN	R W	Channel Enable	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
CH_EN_BW	R W	Channel Enable, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
COMP_EN	R W	Comparator Enable	0x00	-	-	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
COMP_EN_BW	R W	Comparator Enable, Bit Wise	0x00	-	-	-	-	-	-	-	CH x
PRST_CS_OEB_IDLE	R W	CS PAD OEB Preset at IDLE State	0x7F	-	CS_OEB_IDLE[6:0]						
PRST_CS_OUT_IDLE	R W	CS PAD OUT Preset at IDLE State	0x00	-	CS_OUT_IDLE[6:0]						
PRST_CH0_CONN_0	R W	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN0			-	CS0_CONN0		
PRST_CH0_CONN_1	R W		0x00	-	CS3_CONN0			-	CS2_CONN0		
PRST_CH0_CONN_2	R W		0x00	-	CS5_CONN0			-	CS4_CONN0		
PRST_CH0_CONN_3	R W		0x00	-	-			-	-		
PRST_CH1_CONN_0	R W	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN1			-	CS0_CONN1		
PRST_CH1_CONN_1	R W		0x00	-	CS3_CONN1			-	CS2_CONN1		
PRST_CH1_CONN_2	R W		0x00	-	CS5_CONN1			-	CS4_CONN1		
PRST_CH1_CONN_3	R W		0x00	-	-			-	-		

Resister Name	RW	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PRST_CH2_CONN_0	RW	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN2			-	CS0_CONN2		
PRST_CH2_CONN_1	RW		0x00	-	CS3_CONN2			-	CS2_CONN2		
PRST_CH2_CONN_2	RW		0x00	-	CS5_CONN2			-	CS4_CONN2		
PRST_CH2_CONN_3	RW		0x00	-	-			-	-		
PRST_CH3_CONN_0	RW	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN3			-	CS0_CONN3		
PRST_CH3_CONN_1	RW		0x00	-	CS3_CONN3			-	CS2_CONN3		
PRST_CH3_CONN_2	RW		0x00	-	CS5_CONN3			-	CS4_CONN3		
PRST_CH3_CONN_3	RW		0x00	-	-			-	-		
PRST_CH4_CONN_0	RW	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN4			-	CS0_CONN4		
PRST_CH4_CONN_1	RW		0x00	-	CS3_CONN4			-	CS2_CONN4		
PRST_CH4_CONN_2	RW		0x00	-	CS5_CONN4			-	CS4_CONN4		
PRST_CH4_CONN_3	RW		0x00	-	-			-	-		
PRST_CH5_CONN_0	RW	Preset CSx_CONNy[2:0] (x=cs pin index, y=channel index) 3'h1:hi-z 3'h2:L 3'h3:H 3'h4: connect to CVC input 3'h5: connect to active shield driver output Others: OEB_IDLE and OUT_IDLE	0x00	-	CS1_CONN5			-	CS0_CONN5		
PRST_CH5_CONN_1	RW		0x00	-	CS3_CONN5			-	CS2_CONN5		
PRST_CH5_CONN_2	RW		0x00	-	CS5_CONN5			-	CS4_CONN5		
PRST_CH5_CONN_3	RW		0x00	-	-			-	-		
-	RW	-	0x00	-	-			-	-		
-	RW		0x00	-	-			-	-		
-	RW		0x00	-	-			-	-		
-	RW		0x00	-	-			-	-		
PRST_SHIELD_EN	RW	Preset, Active Shield Enable	0x00	-	-	CH5	CH4	CH3	CH2	CH1	CH0
PRST_SHIELD_STR_0	RW	Preset, Active Shield Strengh Channel 0/1/2/3	0x00	CH3		CH2		CH1		CH0	
PRST_SHIELD_STR_1	RW	Preset, Active Shield Strengh Channel 4/5	0x00	-		-		CH5		CH4	
CS_OEB	RW	CS PADs output enable, Active Low	0x7F	CS_OEB[7:0]							

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CS_OUT	R W	CS PADs output value	0x00	-	CS_OUT[6:0]						
CS_AE	R W	CS PADs analog IO enable	0x00	-	CS_AE[6:0]						
IOCNT_A	R W	Preset, Connect CS to Active shield	0x00	-	IOCNT_A[6:0]						
IOCNT_B	R W	Strength Trim[1:0] Active Shield Enable Connect CS[3:0] to BOUT[3:0]	0x00	-	STR_TRIM[1:0]		ACTIVESHIELD_EN	IOCNT_B[3:0]			
IOCNT_C	R W	Connect CS to CVC (or ADC)	0x00	-	IOCNT_C[6:0]						
PRST_AFE_GAIN_CH0	R W	Preset ADC/AFE Gain for Channel 0	0x04	-	-	ADCG	CH0_CGAIN[4:0]				
PRST_AFE_GAIN_CH1	R W	Preset ADC/AFE Gain for Channel 1	0x04	-	-	ADCG	CH1_CGAIN[4:0]				
PRST_AFE_GAIN_CH2	R W	Preset ADC/AFE Gain for Channel 2	0x04	-	-	ADCG	CH2_CGAIN[4:0]				
PRST_AFE_GAIN_CH3	R W	Preset ADC/AFE Gain for Channel 3	0x04	-	-	ADCG	CH3_CGAIN[4:0]				
PRST_AFE_GAIN_CH4	R W	Preset ADC/AFE Gain for Channel 4	0x04	-	-	ADCG	CH4_CGAIN[4:0]				
PRST_AFE_GAIN_CH5	R W	Preset ADC/AFE Gain for Channel 5	0x04	-	-	ADCG	CH5_CGAIN[4:0]				
-	R W	-	0x04	-	-	-	-				
AFE_GAIN	R W	ADC/AFE Gain	0x04	-	-	ADCG	CGAIN[4:0]				
PRST_CVC_D_CH0H	R W	Preset CVC DAC value for Ch0, upper bits	0x00	-	-	CH0_CVC_D[13:8]					
PRST_CVC_D_CH0L	R W	Preset CVC DAC value for Ch0, lower bits	0x00	CH0_CVC_D[7:0]							
PRST_CVC_D_CH1H	R W	Preset CVC DAC value for Ch1, upper bits	0x00	-	-	CH1_CVC_D[13:8]					
PRST_CVC_D_CH1L	R W	Preset CVC DAC value for Ch1, lower bits	0x00	CH1_CVC_D[7:0]							
PRST_CVC_D_CH2H	R W	Preset CVC DAC value for Ch2, upper bits	0x00	-	-	CH2_CVC_D[13:8]					
PRST_CVC_D_CH2L	R W	Preset CVC DAC value for Ch2, lower bits	0x00	CH2_CVC_D[7:0]							
PRST_CVC_D_CH3H	R W	Preset CVC DAC value for Ch3, upper bits	0x00	-	-	CH3_CVC_D[13:8]					
PRST_CVC_D_CH3L	R W	Preset CVC DAC value for Ch3, lower bits	0x00	CH3_CVC_D[7:0]							
PRST_CVC_D_CH4H	R W	Preset CVC DAC value for Ch4, upper bits	0x00	-	-	CH4_CVC_D[13:8]					
PRST_CVC_D_CH4L	R W	Preset CVC DAC value for Ch4, lower bits	0x00	CH4_CVC_D[7:0]							

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PRST_CVC_D_CH5H	R W	Preset CVC DAC value for Ch5, upper bits	0x00	-	-	CH5_CVC_D[13:8]					
PRST_CVC_D_CH5L	R W	Preset CVC DAC value for Ch5, lower bits	0x00	CH5_CVC_D[7:0]							
-	R W	-	0x00	-	-	-					
-	R W	-	0x00	-							
CVC_D_H	R W	CVC DAC value, upper bits	0x00	-	-	CVC_D[13:8]					
CVC_D_L	R W	CVC DAC value, lower bits	0x00	CVC_D[7:0]							
PRST_FS_DSM_CH0	R W	Preset DSM ADC Sampling Frequency for Ch0	0x03	CH0_FS_DSM[7:0]							
PRST_FS_DSM_CH1	R W	Preset DSM ADC Sampling Frequency for Ch1	0x03	CH1_FS_DSM[7:0]							
PRST_FS_DSM_CH2	R W	Preset DSM ADC Sampling Frequency for Ch2	0x03	CH2_FS_DSM[7:0]							
PRST_FS_DSM_CH3	R W	Preset DSM ADC Sampling Frequency for Ch3	0x03	CH3_FS_DSM[7:0]							
PRST_FS_DSM_CH4	R W	Preset DSM ADC Sampling Frequency for Ch4	0x03	CH4_FS_DSM[7:0]							
PRST_FS_DSM_CH5	R W	Preset DSM ADC Sampling Frequency for Ch5	0x03	CH5_FS_DSM[7:0]							
-	R W	-	0x03	-							
AFEC_FS_DSM	R W	DSM ADC Sampling Frequency	0x03	AFEC_FS_DSM[7:0]							
AFEC_FS_CAL	R W	Calibration Sampling Frequency	0x09	AFEC_FS_CAL[7:0]							
PRST_DSM_OSR_0	W	Preset DSM ADC Oversampling Ratio for Ch0	0x55	CH1_DSM_OSR				CH0_DSM_OSR			
PRST_DSM_OSR_1	W	Preset DSM ADC Oversampling Ratio for Ch1	0x55	CH3_DSM_OSR				CH2_DSM_OSR			
PRST_DSM_OSR_2	W	Preset DSM ADC Oversampling Ratio for Ch2	0x55	CH5_DSM_OSR				CH4_DSM_OSR			
-	-	-	-	-				-			
AFEC_DSM_OSR	W	DSM ADC Oversampling Ratio	0x55					AFEC_DSM_OSR			
AFEC_CLK_PH	R W	Conversion and Calibration Clock Phase Register	0x44	CAL_PH2		CAL_PH1		CONV_PH2		CONV_PH1	
AFEC_SAR_CFG	R W	SAR ADC Configuration FS_SAR: Sampling Frequency, 16 MHz/ (2^ FS_SAR) SMPL_LEN: Sampling Duration, 0=1.5 µs, 1 = 3 µs SMPL_NEG: Sampling clock edge selection, 0 = positive edge, 1 = negative edge DUMMY_EN: Dummy Sampling Enable, 0 = disable, 1 = enable	0x00	-	-	-	DUMMY_EN	SAMPLE_NEG	SAMPLE_LEN	FS_SAR	
AFEC_DSM_OFFSET_H	R W	DSM_OFFSET: DSM ADC offset compensation, -2048 ~ 2047	0x00	-	-	-	-	DSM_OFFSET[11:8]			

Resister Name	R W	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
AFEC_DSM_OFFSET_L	R W		0x00	DSM_OFFSET[7:0]							
AFEC_DSM_GAIN_H	R W	DSM_GAIN: b'0.0000000000 ~ b'1.1111111111	0x04-	-	-	-	-	-	GAIN[10:8]		
AFEC_DSM_GAIN_L	R W		0x00	GAIN[7:0]							
AFEC_SAR_OFFSET_H	R W	SAR_OFFSET: SAR ADC offset compensation, -2048 ~ 2047	0x00	-	-	-	-	SAR_OFFSET[11:8]			
AFEC_SAR_OFFSET_L	R W		0x00	SAR_OFFSET[7:0]							
AFEC_SAR_GAIN_H	R W	SAR_GAIN: b'0.0000000000 ~ b'1.1111111111	0x04	-	-	-	-	-	GAIN[10:8]		
AFEC_SAR_GAIN_L	R W		0x00	GAIN[7:0]							
CMD	W	CMD_LOAD_PRESET [7:0] = b'00, Write, Load values on preset registers to specific registers AFE: '1' – load presets to AFE_GAIN, CVC_D, FS_DSM, DSM_OSR registers CS: '1' load presets to CS_OEB, CS_OUT, CS_AE, A, C, SHIELD_STR registers CS_IDLE: '1' – load presets CS_OEB_IDLE, CS_OUT_IDLE to CS_OEB, CS_OUT and load 0 to CS_AE, A, C CMD_CONVERSION [7:0] = b'10, Write Do signal read CMD_CALIBRATION [7:0] = b'11, Write Do calibration read DMA_EN: DMA enable, 0: disable, 1:enable DMA_BE: DMA begin 1: begin INT_EN: Interrupt enable 0: disable, 1: enable	0x00	0	0	AFE	CS	CS_IDLE	CH_NUM		
	W		0x00	1	0	DMA_EN	DMA_BE	INT_EN	SDLY		
	W		0x00	1	1	DMA_EN	DMA_BE	INT_EN	SDLY		
	R		0x00	0	0	0	0	0	0	0	BUSY
AFEC_DMA_ADDR_H	R W	DMA_ADDR: DMA address	0x00	DMA_ADDR[15:8]							
AFEC_DMA_ADDR_L	R W		0x00	DMA_ADDR[7:0]							
AFEC_ADCOUT_3	R O	ADC Data Output	0x00	ADCOUT[31:24]							
AFEC_ADCOUT_2	R O		0x00	ADCOUT[23:16]							
AFEC_ADCOUT_1	R O		0x00	ADCOUT[15:8]							
AFEC_ADCOUT_0	R O		0x00	ADCOUT[7:0]							

Resister Name	RW	Description	Default	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
AFEC_DSMACC_3	RO	DSM ADC DATA Accumulation Output	0x00	DSMACC[31:24]							
AFEC_DSMACC_2	RO		0x00	DSMACC[23:16]							
AFEC_DSMACC_1	RO		0x00	DSMACC[15:8]							
AFEC_DSMACC_0	RO		0x00	DSMACC[7:0]							
AFEC_SARACC_H	RO	SAR ADC DATA Accumulation Output	0x00	SARACC[15:8]							
AFEC_SARACC_L	RO		0x00	SARACC[7:0]							
AFEC_CALRESULT_H	RO	Calibration Result Output	0x00	0	0	CALRESULT[13:8]					
AFEC_CALRESULT_L	RO		0x00	CALRESULT[7:0]							
AFE_BLK_EN	RW	AFE Block Control ADC_SEL: ADC Input Selection 0: CVC, 1: PAD, 2: TS, 3: (VDDD,VCOM) TS_PDB: TS power control, 0: power down, 1: power up DS_PDB: DSM ADC power control, 0: power down, 1: power up CAL_PDB: Calibrator power control, 0: power down, 1: power up CVC_PDB: CVC power control, 0: power down, 1: power up BIASGEN_PDB: bias generator power control 0: power down, 1: power up	0x00	-	ADC_SEL[1:0]		TS_PDB	DS_PDB	CAL_PDB	CVC_PDB	BIASGEN_PDB

11 Applications

11.1 Typical Application

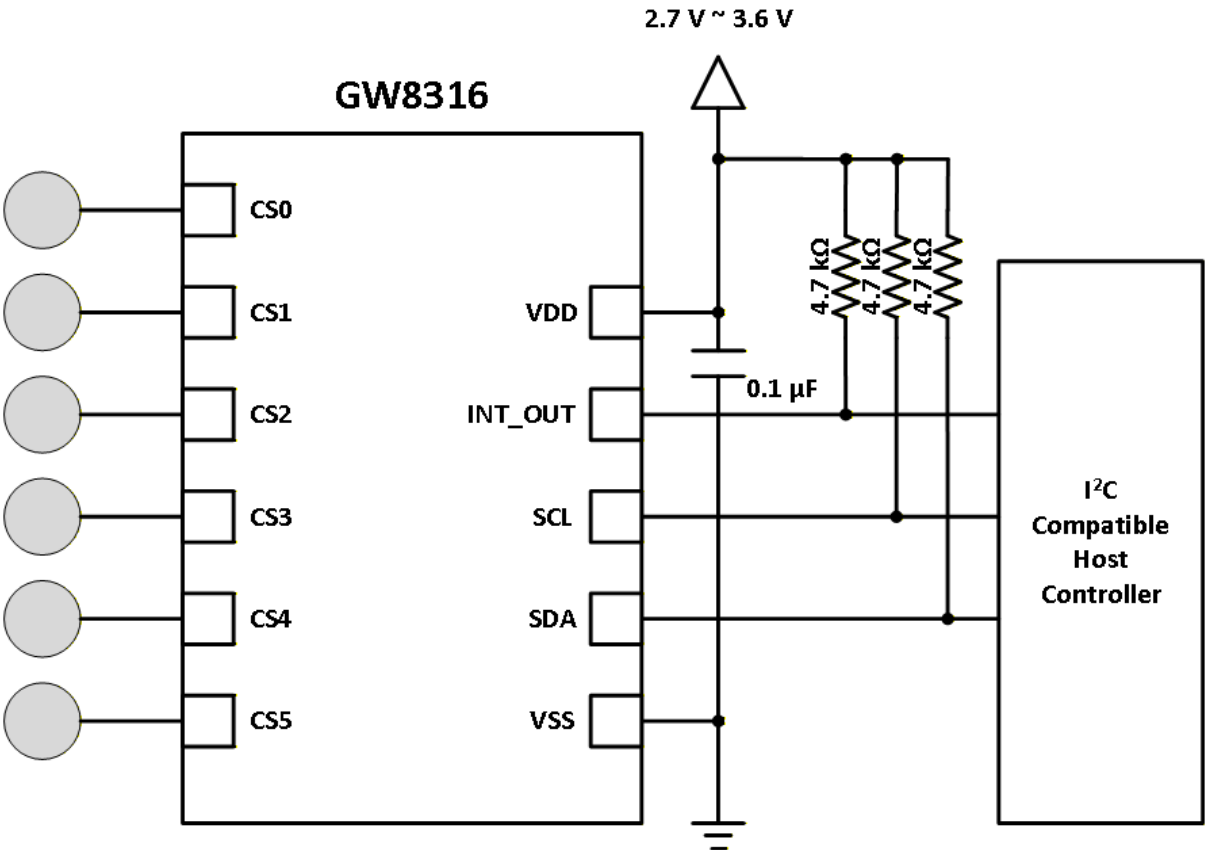


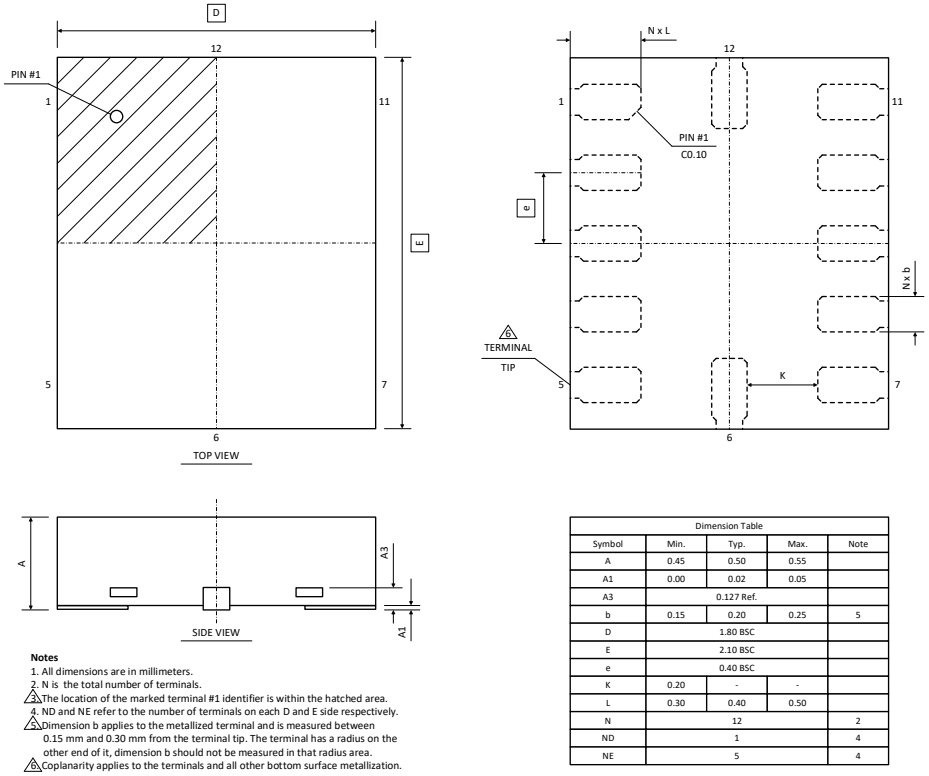
Figure 6 Typical Application Example

11.2 Guidelines for external component selection

Symbol	Description	Note	MIN	TYP	MAX	UNIT
C_{VDD}	Supply Voltage Decoupling Capacitor	Min X5R type Min 6.3V rating		0.1		µF
R_{PULLUP}	Host Interface Pull-up Resistors			4.7		kΩ

12 Package Information

12 DFN Package

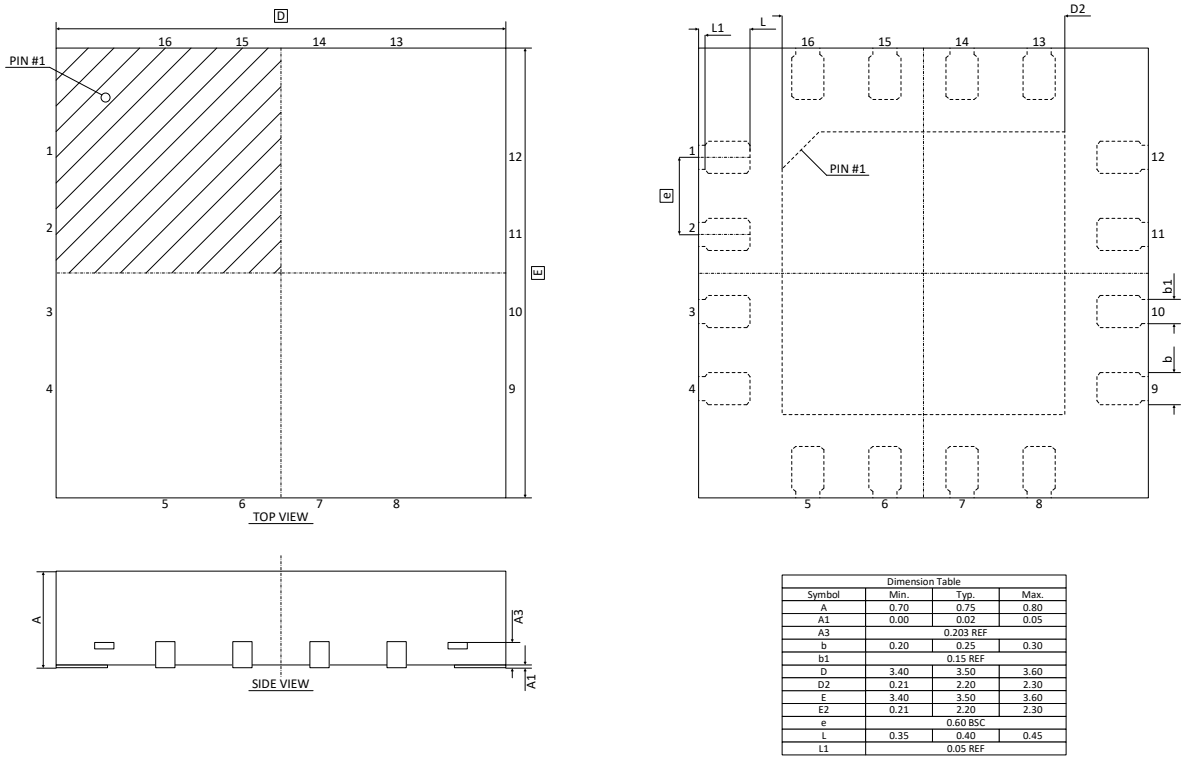


Dimension Table				
Symbol	Min.	Typ.	Max.	Note
A	0.45	0.50	0.55	
A1	0.00	0.02	0.05	
A3		0.127 Ref.		
b	0.15	0.20	0.25	5
D		1.80 BSC		
E		2.10 BSC		
e		0.40 BSC		
K	0.20	-	-	
L	0.30	0.40	0.50	
N		12		2
ND		1		4
NE		5		4

Notes

1. All dimensions are in millimeters.
2. N is the total number of terminals.
3. The location of the marked terminal #1 identifier is within the hatched area.
4. ND and NE refer to the number of terminals on each D and E side respectively.
5. Dimension b applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. The terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
6. Coplanarity applies to the terminals and all other bottom surface metallization.

16 QFN Package



Dimension Table			
Symbol	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
b1		0.15 REF	
D	3.40	3.50	3.60
D2	0.21	2.20	2.30
E	3.40	3.50	3.60
E2	0.21	2.20	2.30
e		0.60 BSC	
L	0.35	0.40	0.45
L1		0.05 REF	

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